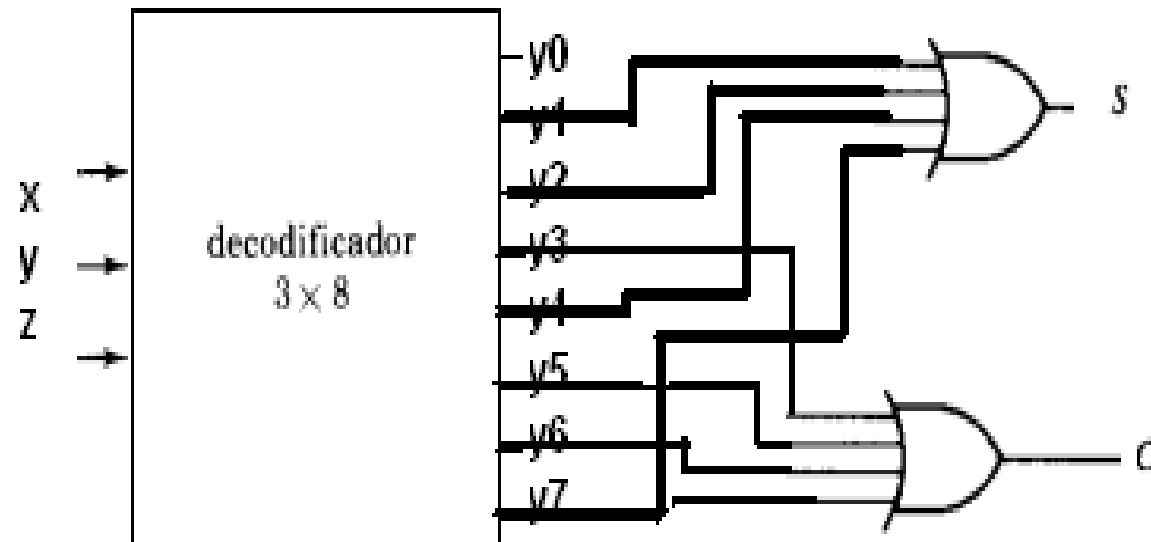


Examen 3 Contestado

FCHE2011

1) Decodificador 3x8 para tabla de sumador completo

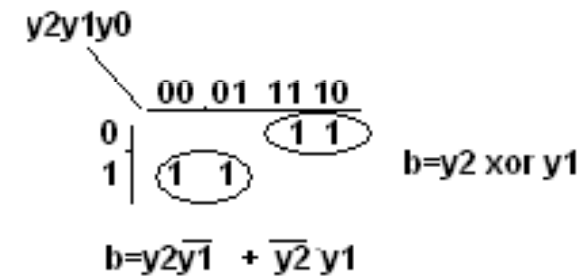
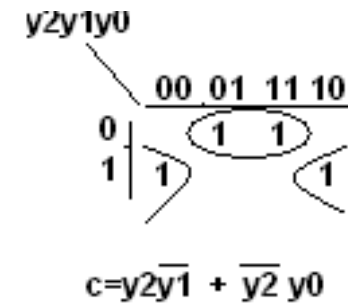
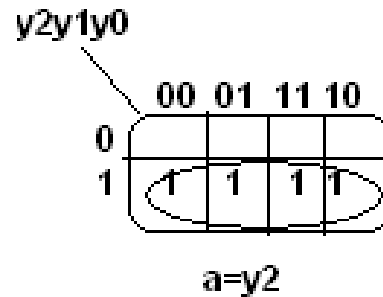
x	y	z	C	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



x	y	z	C	s
0	0	0	0 · y_0	0
0	0	1	0 · y_1	1
0	1	0	0 · y_2	1
0	1	1	1 · y_3	0
1	0	0	0 · y_4	1
1	0	1	1 · y_5	0
1	1	0	1 · y_6	0
1	1	1	1 · y_7	1

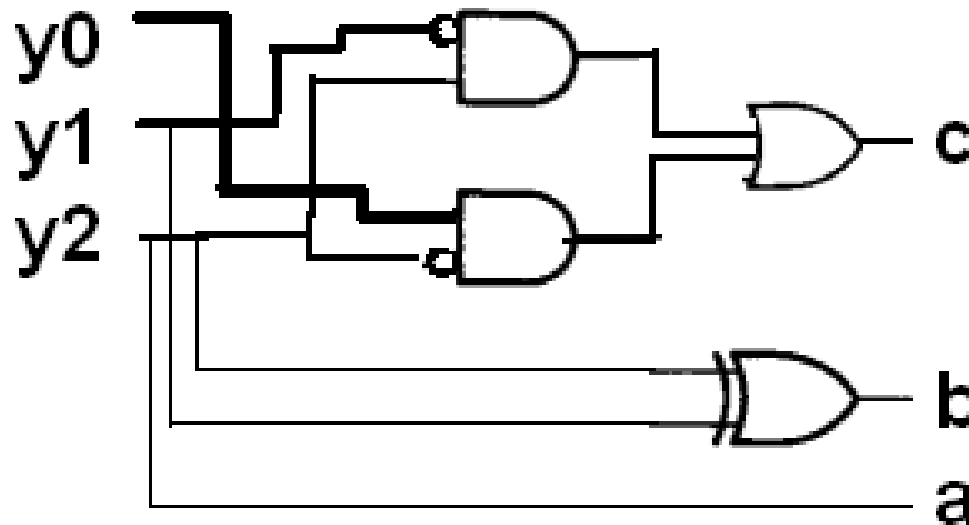
2) Realiza circuito Codificador BCD/GRAY

x	y	z	a	b	c
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

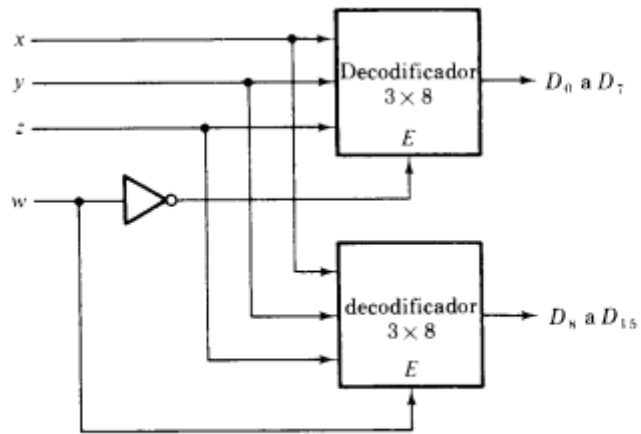


ab	f
00	0
01	1
10	1
11	0

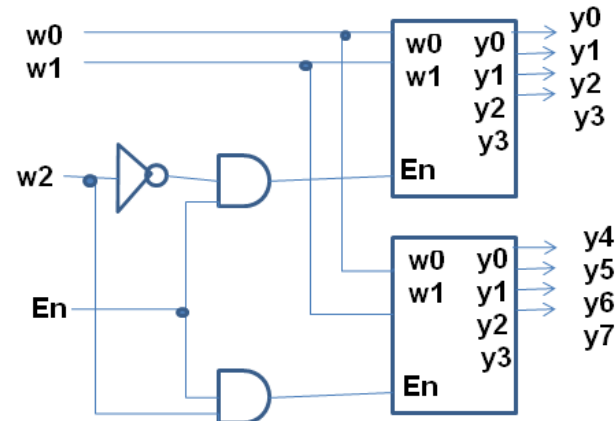
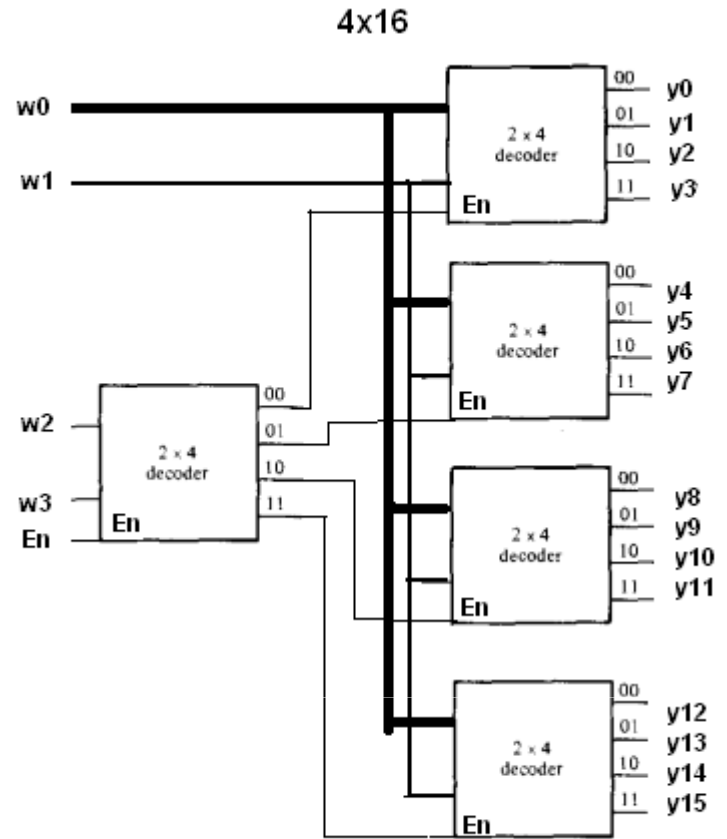
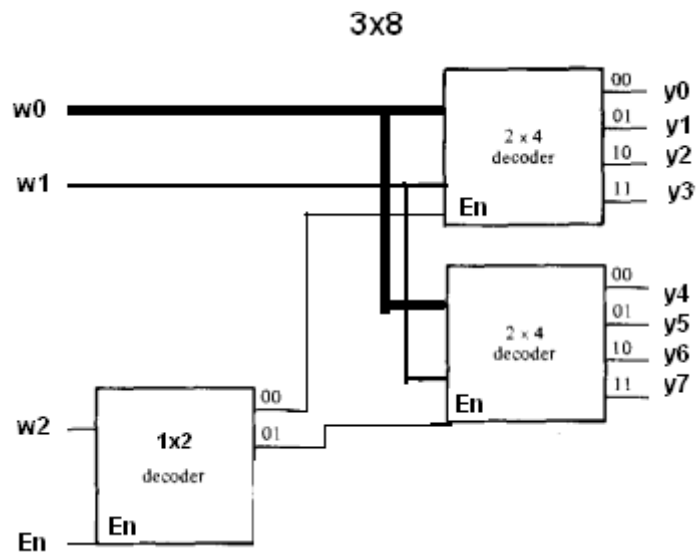
$f = a \text{ xor } b$
 $\bar{a}b + a\bar{b}$



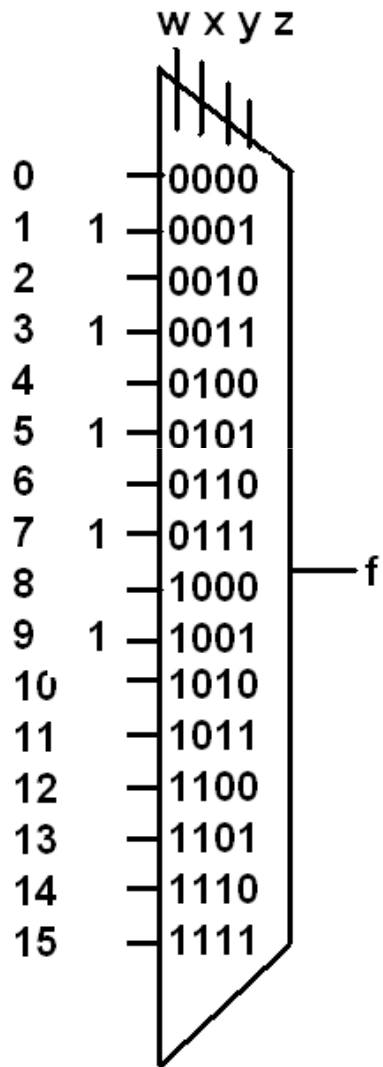
3). DECODIFICADORES



Un decodificador de 4 × 16 construido con dos decodificadores de 3 × 8

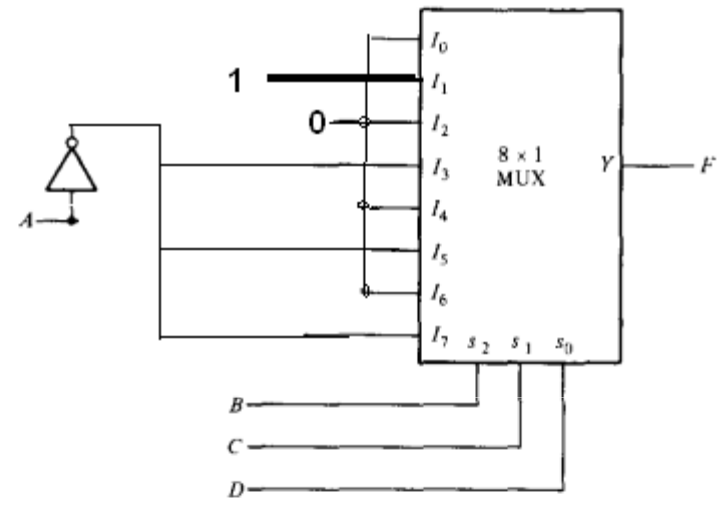


4) Multiplexor $f(w,x,y,z) = \text{Sum}(1,3,5,7,9)$



A	BCD	f
0	0 000	0
1	0 001	1
2	0 010	0
3	0 011	1
4	0 100	0
5	0 101	1
6	0 110	0
7	0 111	1
8	1 000	0
9	1 001	1
10	1 010	0
11	1 011	0
12	1 100	0
13	1 101	0
14	1 110	0
15	1 111	0

	10	11	12	13	14	15	16	17
A'	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	0	1	0	A'	0	A'	0	A'



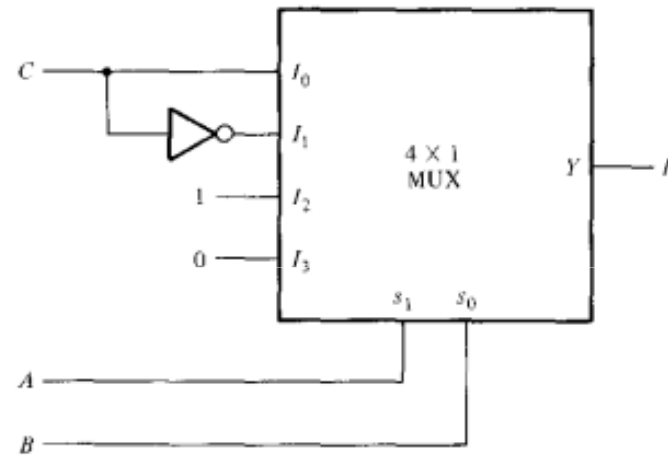
A=0				A=1			
A	BCD	f		A	BCD	f	
0	0 000	0		8	1 000	0	$10 = 0$
1	0 001	1		9	1 001	1	$11 = 1$
2	0 010	0		10	1 010	0	$12 = 0$
3	0 011	1		11	1 011	0	$13 = A'$
4	0 100	0		12	1 100	0	$14 = 0$
5	0 101	1		13	1 101	0	$15 = A'$
6	0 110	0		14	1 110	0	$16 = 0$
7	0 111	1		15	1 111	0	$17 = A'$

¿Como se hace?

$$F(A, B, C) = \Sigma(1, 2, 4, 5)$$

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(a) Truth table



(b) Multiplexer implementation

	I_0	I_1	I_2	I_3
C'	0	2	4	6
C	1	3	5	7
	C	C'	1	0

(c) Implementation table

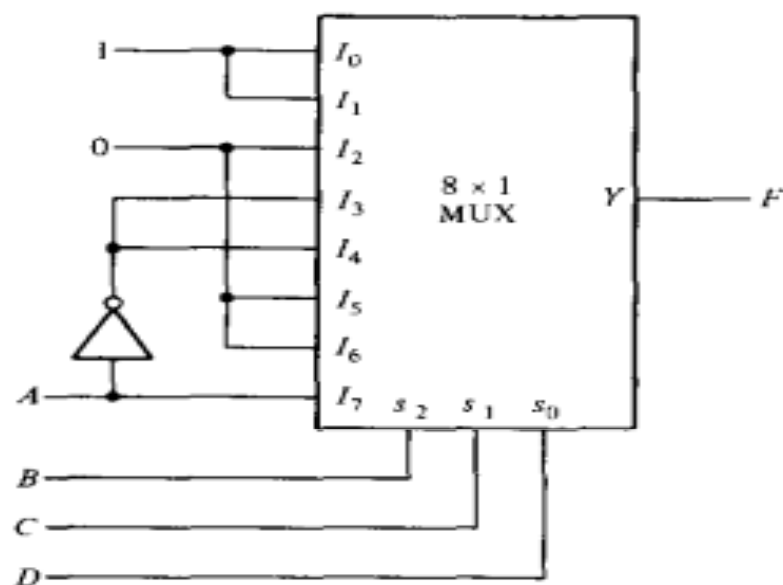
Implementing $F(A, B, C) = \Sigma(1, 2, 4, 5)$ with a multiplexer

Implement the following function with a multiplexer:

$$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$$

This is a four-variable function and, therefore, we need a multiplexer with three selection lines and eight inputs. We choose to apply variables B , C , and D to the selection lines. The implementation table is then as shown in Fig. 5-20. The first half of the

	A	BCD	
0	0	000	1
1	0	001	1
2	0	010	
3	0	011	1
4	0	100	1
5	0	101	
6	0	110	
7	0	111	
8	1	000	1
9	1	001	1
10	1	010	
11	1	011	
12	1	100	
13	1	101	
14	1	110	
15	1	111	1



	A	BCD			A	BCD			
0	0	000	1	8	1	000	1	10 = 1	
1	0	001	1	9	1	001	1	11 = 1	
2	0	010		10	1	010		12 = 0	
3	0	011	1	11	1	011		13 = A'	
4	0	100	1	12	1	100		14 = A'	
5	0	101		13	1	101		15 = 0	
6	0	110		14	1	110		16 = 0	
7	0	111		15	1	111	1	17 = A	
A=0				A=1					

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	①	②	3	④	⑤	6	7	
A	⑧	⑨	10	11	12	13	14	⑮
	1	1	0	A'	A'	0	0	A

5) Tablas de verdad y circuito FF: sr,jk,d,t

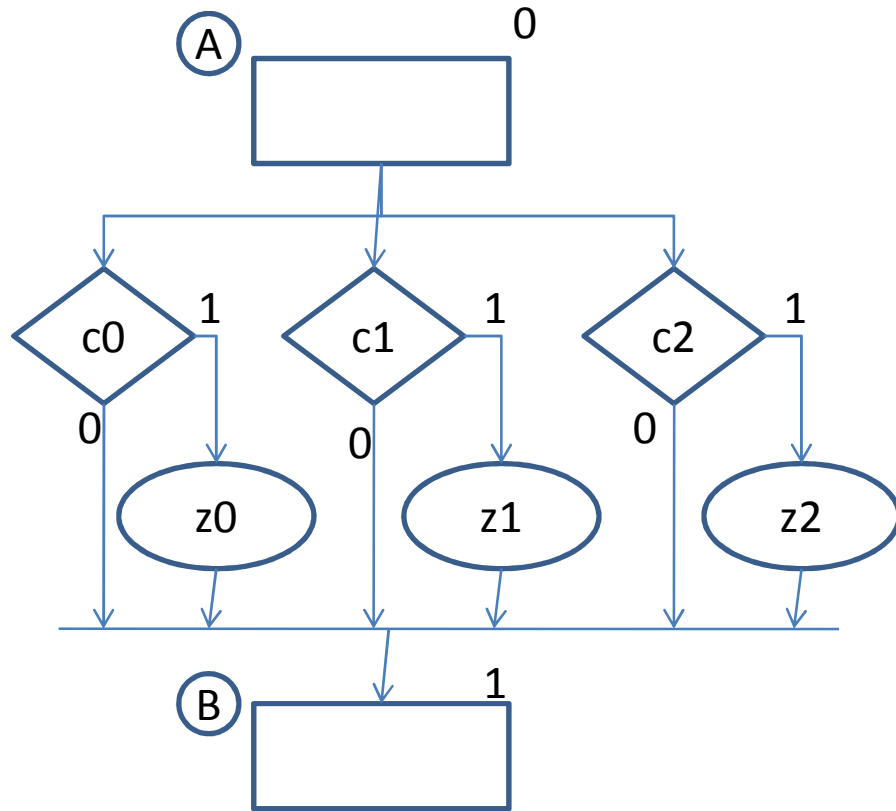
Flip-Flop Characteristic Tables

JK Flip-Flop			RS Flip-Flop		
J	K	$Q(t+1)$	S	R	$Q(t+1)$
0	0	$Q(t)$ No change	0	0	$Q(t)$ No change
0	1	0 Reset	0	1	0 Reset
1	0	1 Set	1	0	1 Set
1	1	$Q'(t)$ Complement	1	1	? Unpredictable

D Flip-Flop			T Flip-Flop		
D	$Q(t+1)$		T	$Q(t+1)$	
0	0	Reset	0	$Q(t)$	No change
1	1	Set	1	$Q'(t)$	Complement

Q	Q+1	D	Q	Q+1	T	Q	Q+1	J	K
0	0	0	0	0	0	0	0	0	X
0	1	1	0	1	1	0	1	1	X
1	0	0	1	0	1	1	0	X	1
1	1	1	1	1	0	1	1	X	0

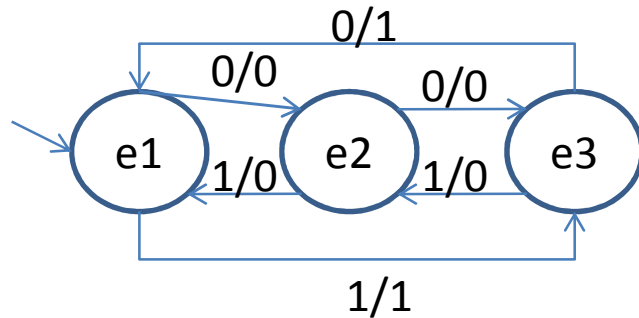
6) Obtén tabla de transición



Q	Entrada	Q+1	Salida
q0	c2c1c0	q0	z0z1z2
A	000	1	1 1 1
	111	1	0 0 0
B	xxx	0	0 0 0

Q	Entrada	Q+1	Salida
q0	c2c1c0	q0	z0z1z2
A	0 x x	1	0 0 1
	x 0 x		0 1 0
	x x 0		1 0 0
A	1 x x	1	0 0 0
	x 1 x		0 0 0
	x x 1		0 0 0
B	xxx	0	0 0 0

7) Diagrama de estados y transiciones contador asc $x=0$ contador desc $x=1$, 2bits



Q	Q+1		Salida	
	x=0	x=1	x=0	x=1
00	01	10	0	1
01	10	00	0	0
10	00	01	1	0

	Q	Entrada x	Q+1	Salida
e1	00	0	01	0
	00	1	10	0
e2	01	0	10	0
	01	1	00	0
e3	10	0	00	1
	10	1	01	1

8) Dado 7) realizar Circuito JK ó D

	Q	Entrada x	Q+1	Salida
e1	00	0	01	0
	00	1	10	0
e2	01	0	10	0
	01	1	00	0
e3	10	0	00	1
	10	1	01	1

Q	Q+1	D	Q	Q+1	T	Q	Q+1	J	K
0	0	0	0	0	0	0	0	0	X
0	1	1	0	1	1	0	1	1	X
1	0	0	1	0	1	1	0	X	1
1	1	1	1	1	0	1	1	X	0

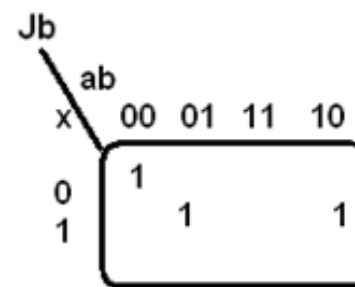
Q	Q+1		Salida	
	x=0	x=1	x=0	x=1
00	01	10	0	1
01	10	00	0	0
10	00	01	1	0

	Salida s	Entrada x	Q ab	Q+1 y1 y2	JaKa	JbKb
e1	0	0	00	01	0 X	1 X
	0	1	00	10	1 X	0 X
e2	0	0	01	10	1 X	0 X
	0	1	01	00	0 X	X 1
e3	1	0	10	00	X 1	0 X
	1	1	10	01	X 1	1 X

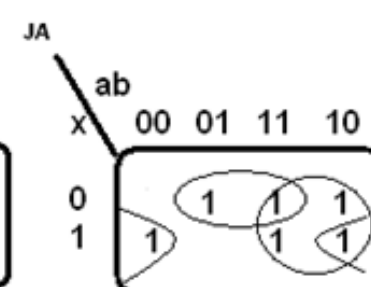
Q ab	Q+1		x=0				x=1				Salida	
	x=0 y1 y2	x=1 y1 y2	ja	ka	jb	kb	ja	ka	jb	kb	x=0	x=1
00	01	10	0	x	1	x	1	x	0	x	0	1
01	10	00	1	x	x	1	0	x	x	1	0	0
10	00	01	x	1	0	x	x	1	1	x	1	0

ka=kb=1

Ka=Kb=1



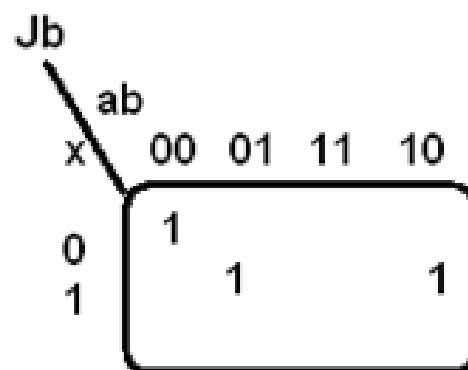
$Jb = x'a'b' + xa'b + xab'$



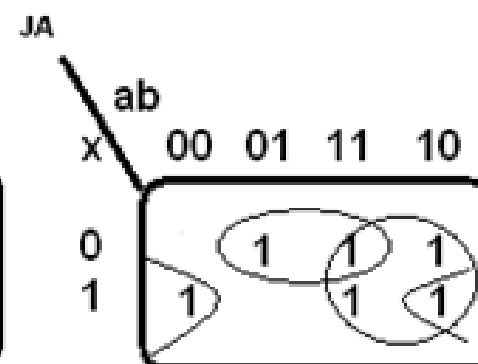
$Ja = xb' + a + x'b$

	Salida s	Entrada x	Q ab	Q+1 y1 y2	JaKa	JbKb
e1	0	0	00	01	0 x	1 x
	0	1	00	10	1 x	0 x
e2	0	0	01	10	1 x	0 x
	0	1	01	00	0 x	x 1
e3	1	0	10	00	x 1	0 x
	1	1	10	01	x 1	1 x

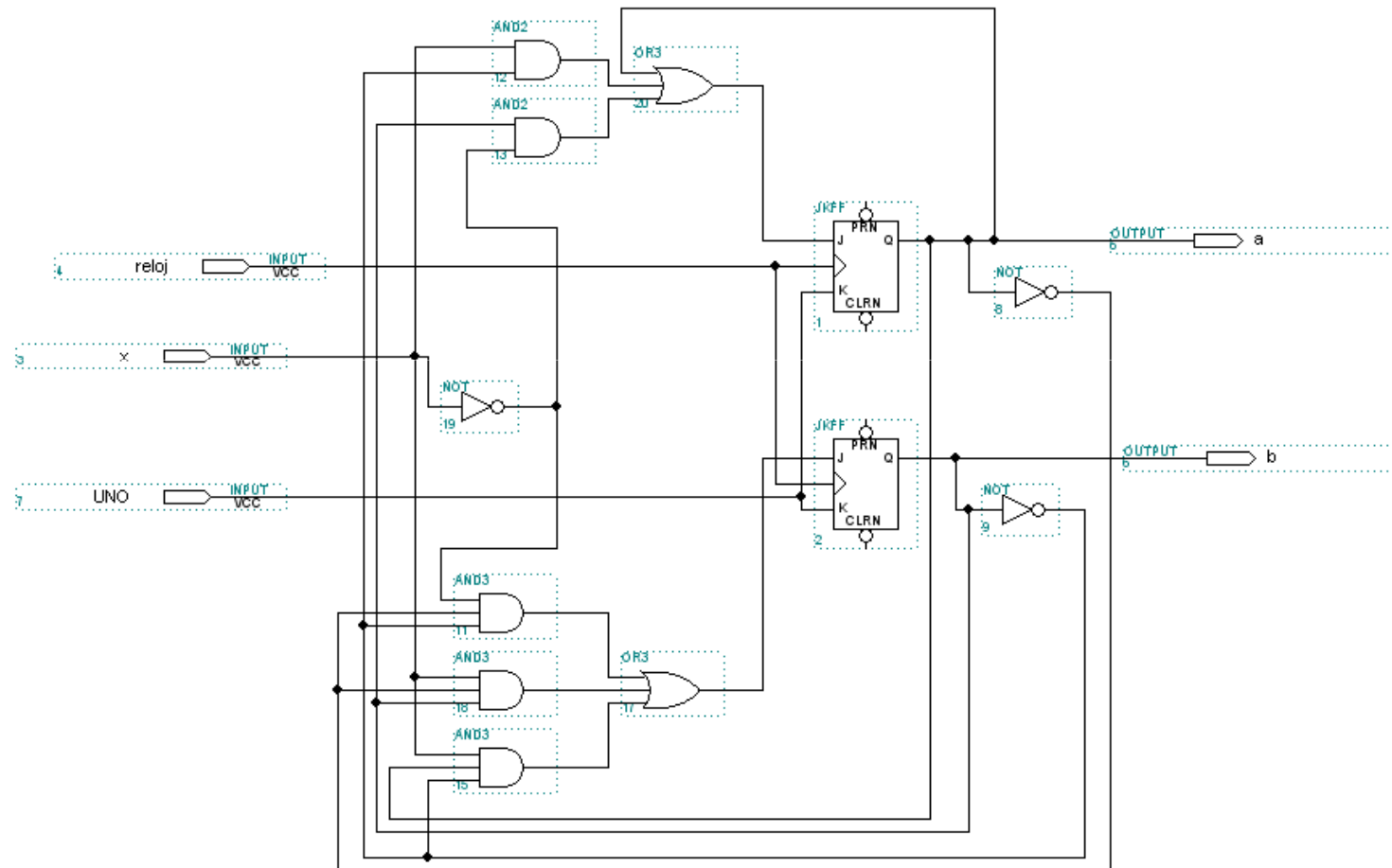
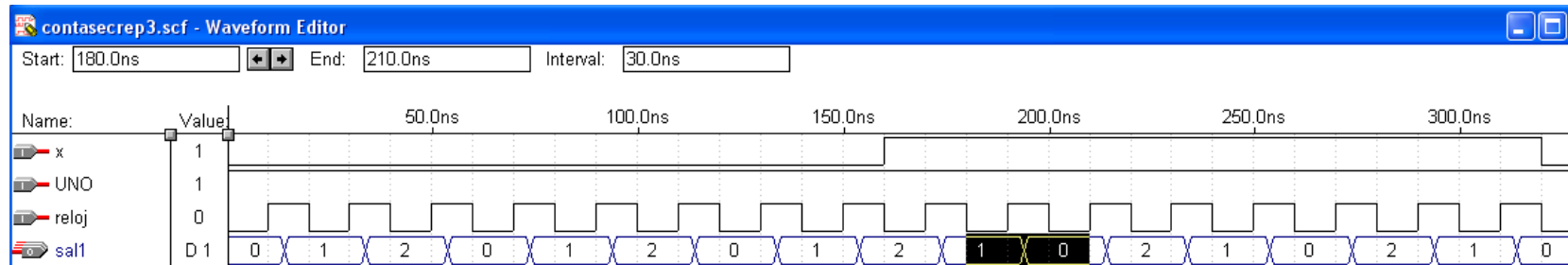
$$K_a = K_b = 1$$



$$J_b = x'a'b' + xa'b + xab'$$



$$J_a = xb' + a + x'b$$



FFD

Entrada		Q	Q+1	D1	D2
x		y2y1	Y2Y1		
0	e1	00	01	0	1
1		00	10	1	0
0	e2	01	10	1	0
1		01	00	0	0
0	e3	10	00	0	0
1		10	01	0	1

Q	Q+1	D
0	0	0
0	1	1
1	0	0
1	1	1

$$z = y2$$

x		y2y1
		00 01 11 10
0		1
1		1

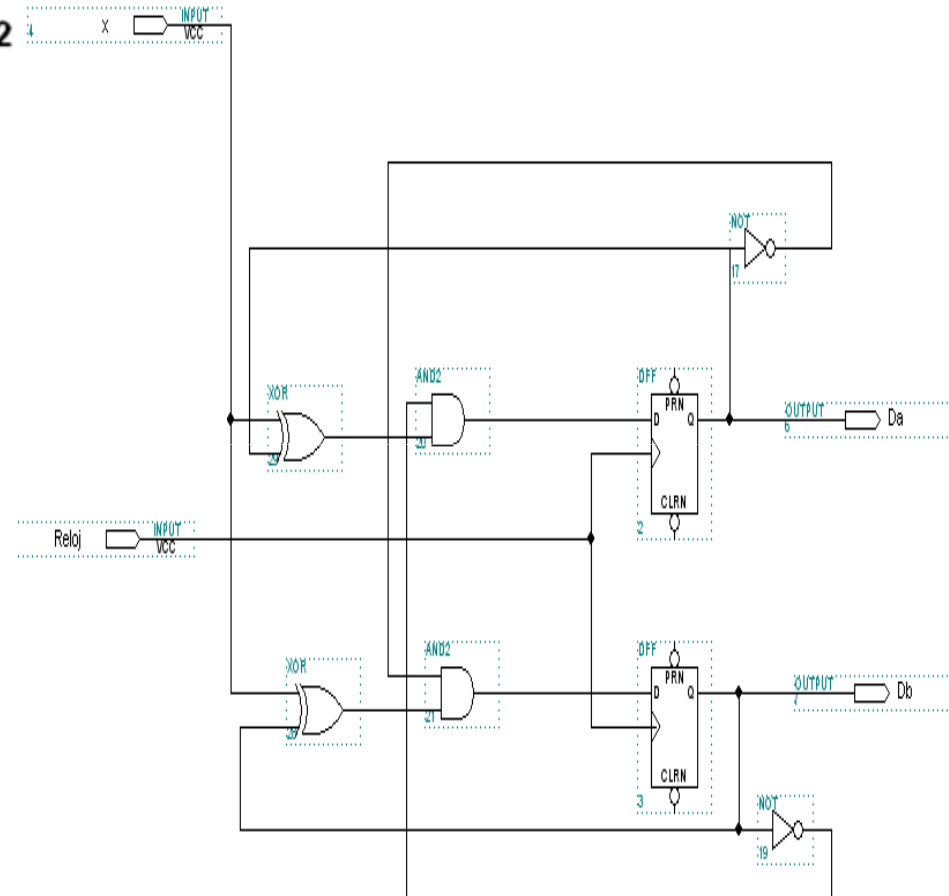
$$D1 = x'y2'y1 + xy2'y1' = y2'(x \oplus y1)$$

x		y2y1
		00 01 11 10
0		1
1		1

$$D2 = x'y2'y1' + xy2y1'$$

$$y1'(x \oplus y2)$$

Q	Q+1		Salida	
	x=0	x=1	x=0	x=1
00	01	10	0	1
01	10	00	0	0
10	00	01	1	0

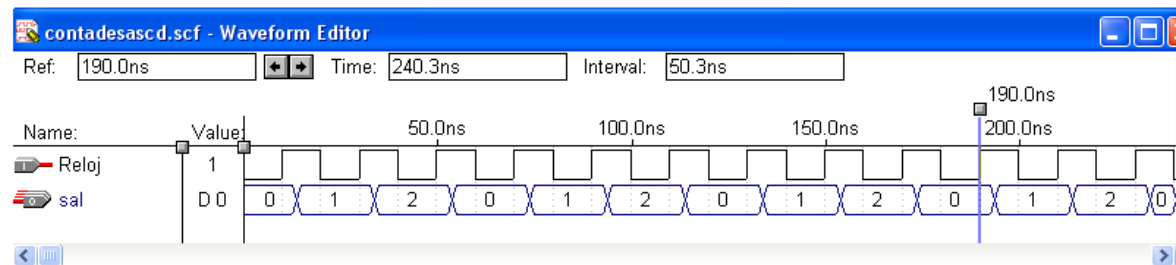
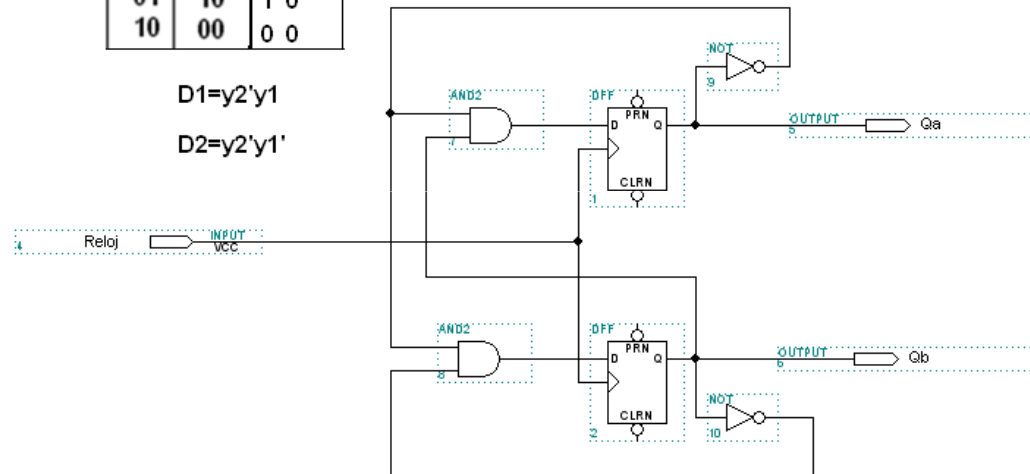


Solo para contador Ascendente

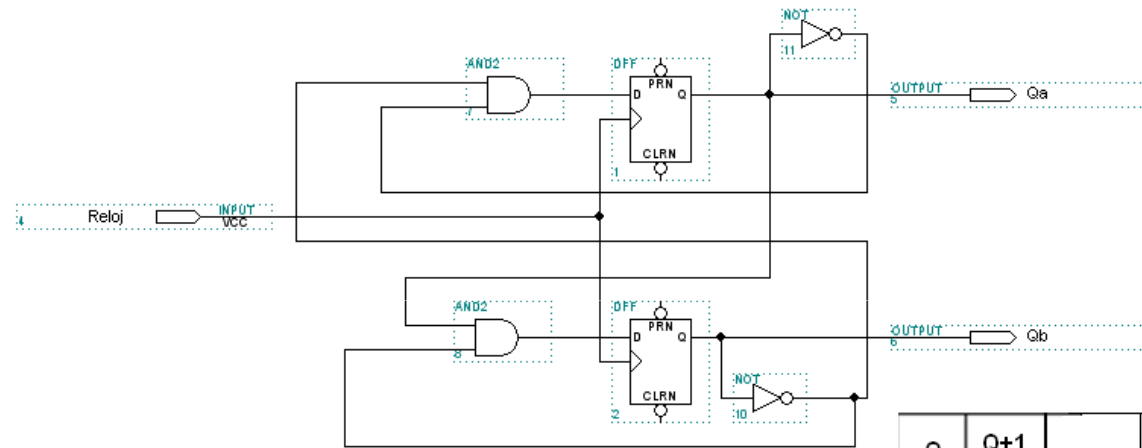
Q	Q+1	
y ₂ y ₁	Y ₂ Y ₁	D ₁ D ₂
00	01	0 1
01	10	1 0
10	00	0 0

$$D1=y_2'y_1$$

$$D2=y_2'y_1'$$



Solo descendente

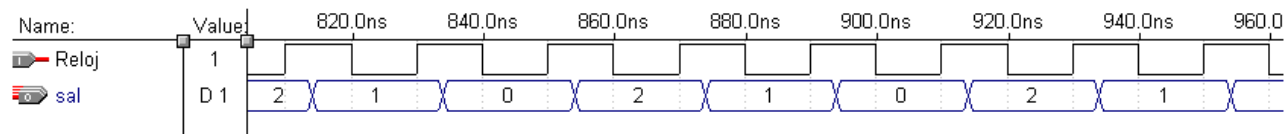


Q	Q+1	D1	D2
y1y2	Y2Y1		
00	10	10	
10	01	01	
01	00	00	

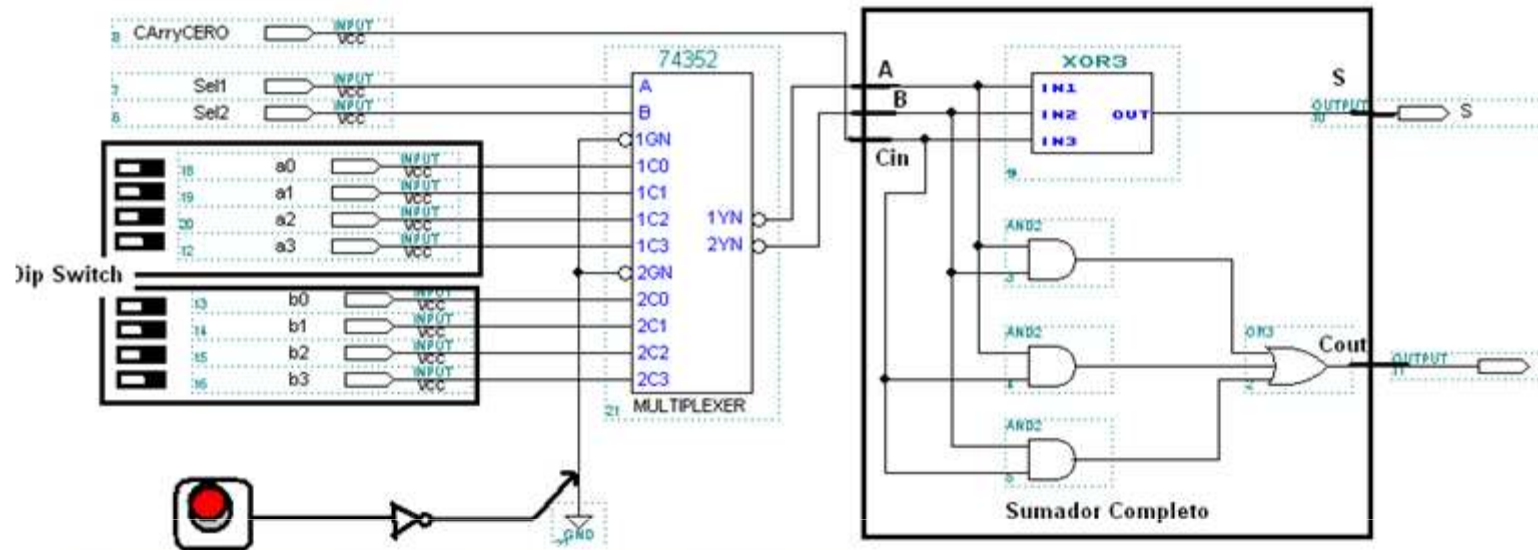
$$D1 = y1'y2'$$

$$D2 = y1y2'$$

Start: 0.0ns End: 1.0us Interval: 1.0us



9) Arma circuito. Suma bit a)



Ref: 826.2ns Time: 868.0ns Interval: 41.8ns

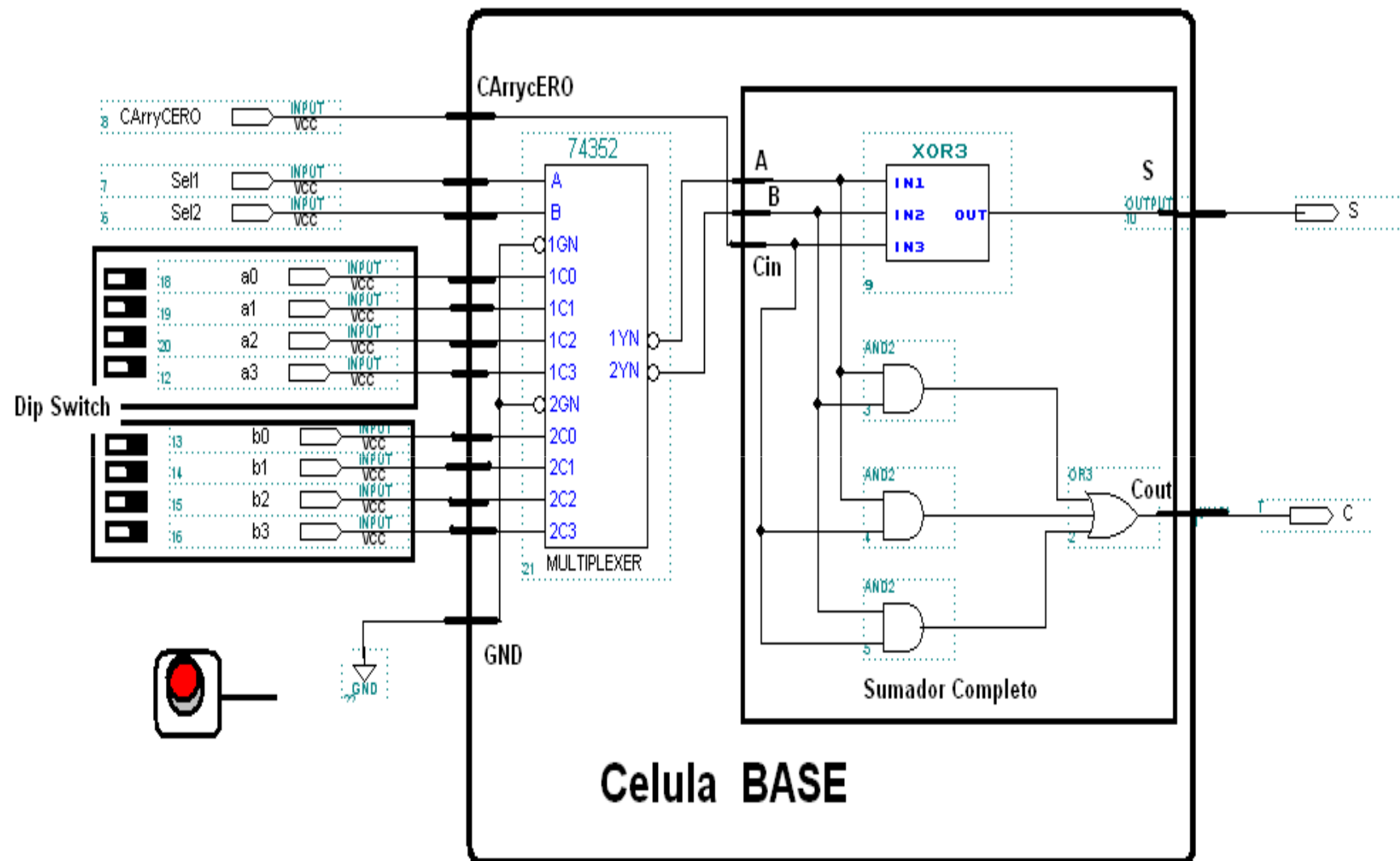
Name:	Value:	820.0ns	840.0ns	860.0ns	880.0ns
Sel2	1				
Sel1	0				
CARRYCERO	0				
b3	1				
b2	0				
b1	1				
b0	0				
a3	0				
a2	0				
a1	1				
a0	1				
S	0				

Sel1	Sel2	Inputs		C	S
		a0	b0		
0	0	1	0	0	1
0	1	a1	b1	1+1	1
		1	1		
1	0	a2	b2	0	0
		0	0		
1	1	a3	b3	0	1
		0	1		

FUNCTION 74352 (b, a, 1gn, 1c[0..3], 2gn, 2c[0..3])
RETURNS (1yn, 2yn):

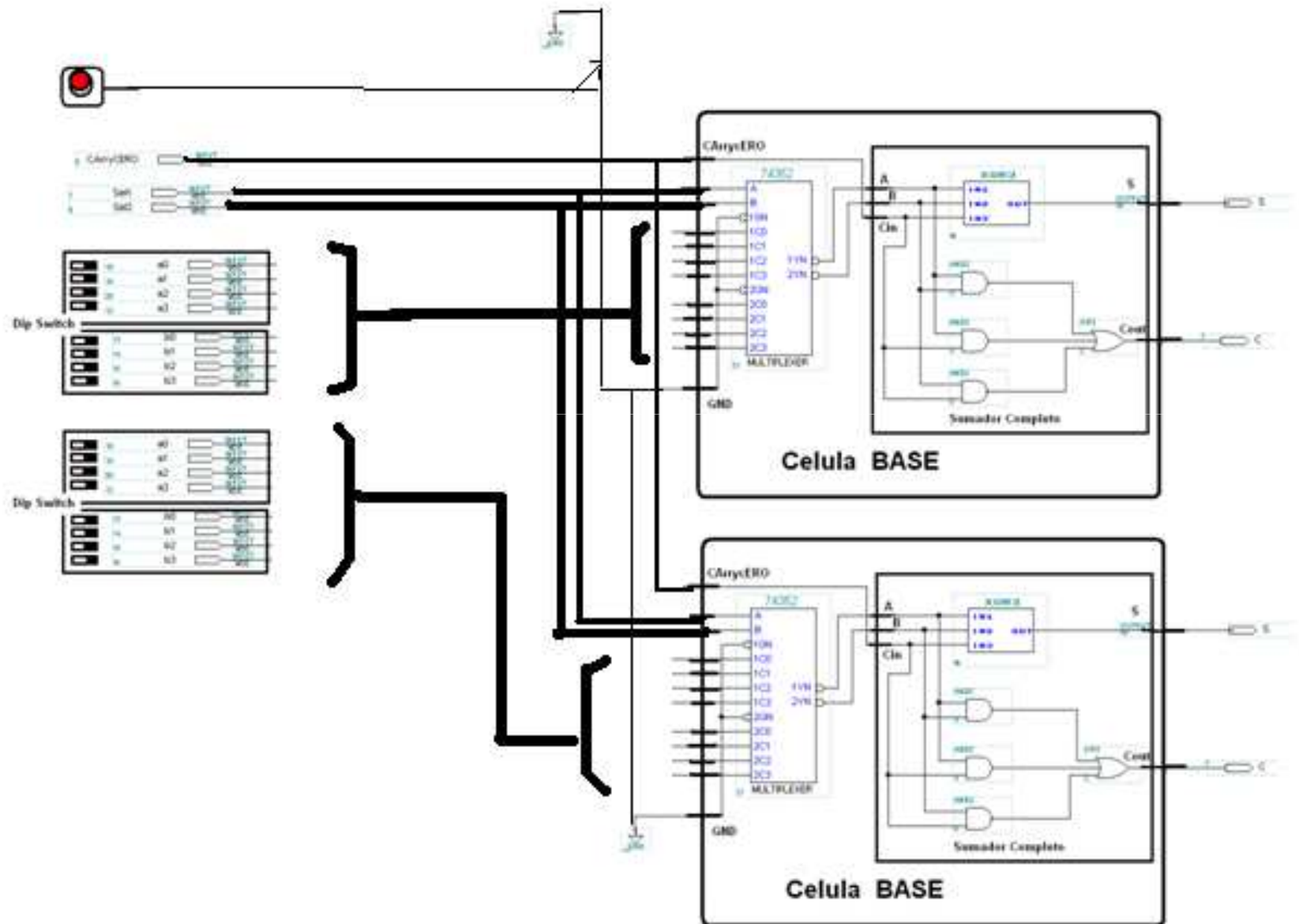
GN	B	A	Inputs				Output
			C0	C1	C2	C3	
H	X	X	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
L	L	H	X	L	X	X	H
L	L	H	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
L	H	H	X	X	X	L	H
L	H	H	X	X	X	H	L

Sumador serial.
Vel. baja,
económico

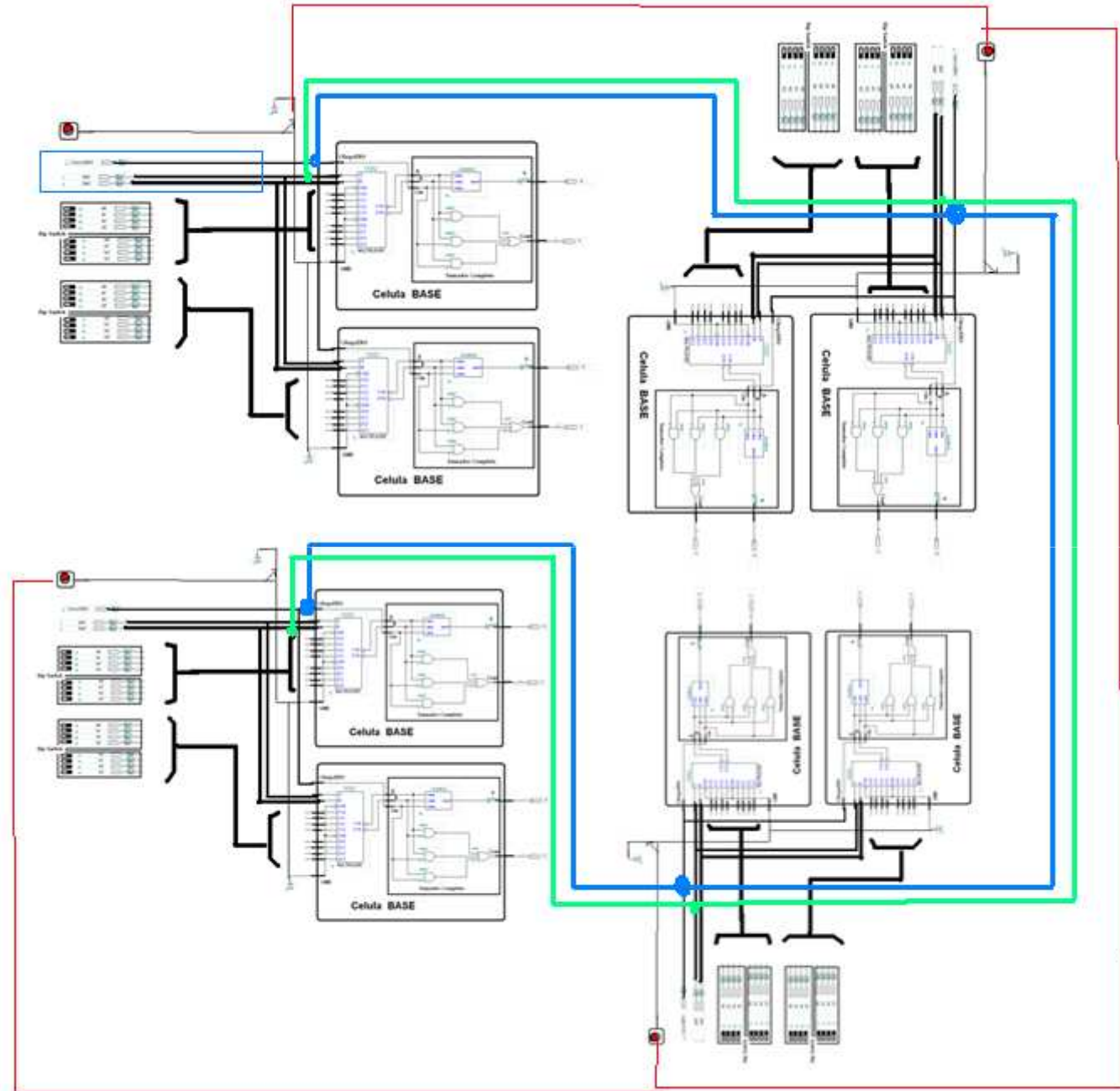


Celula BASE

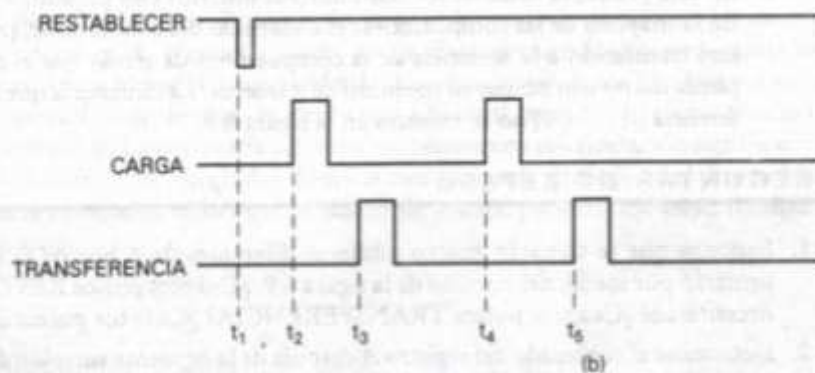
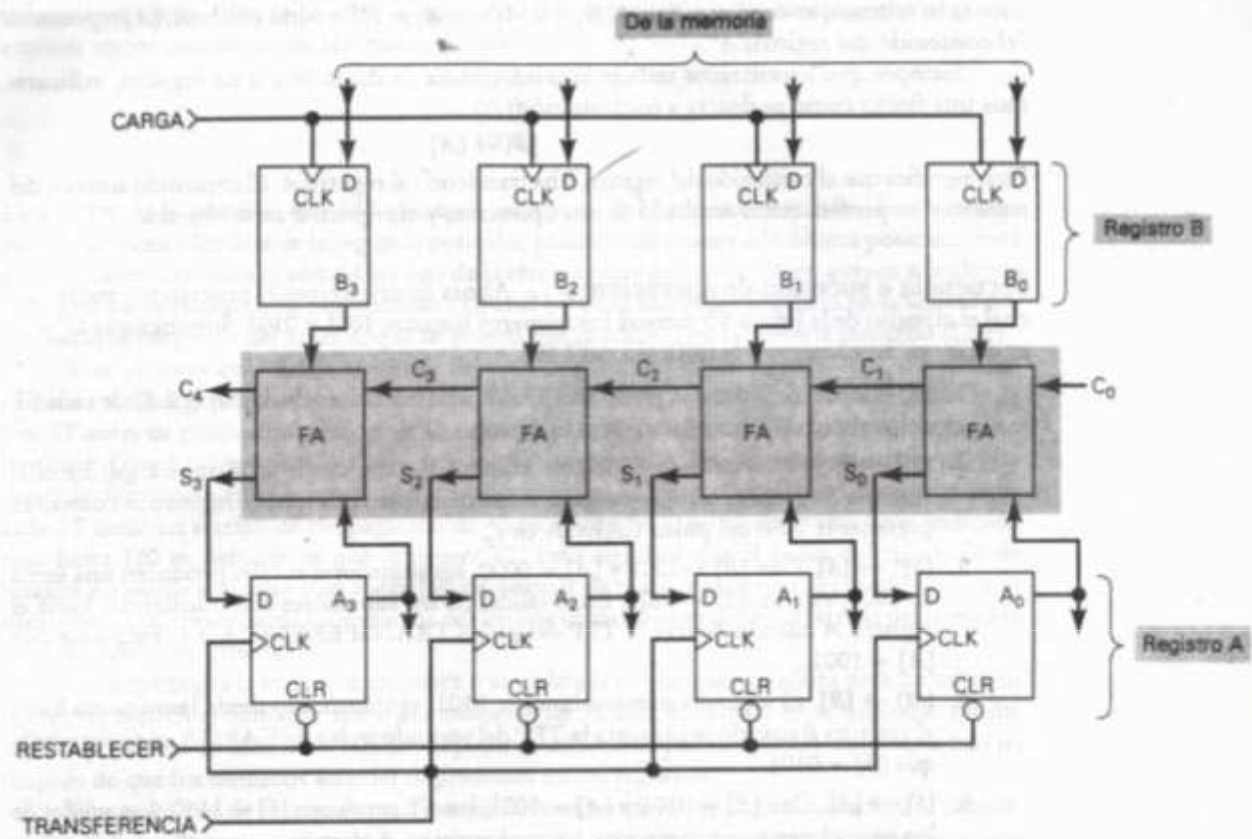
9.b)



9.c)

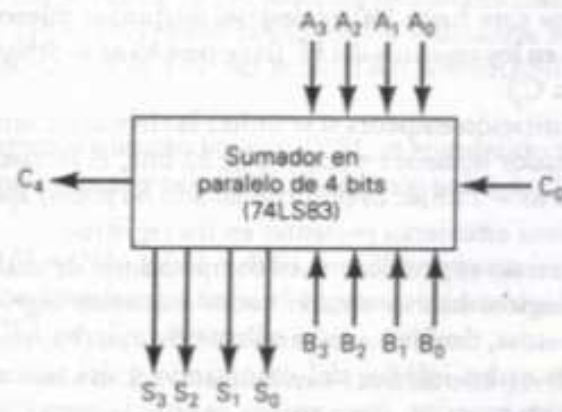


Sumador
cuasi-paralelo
económico

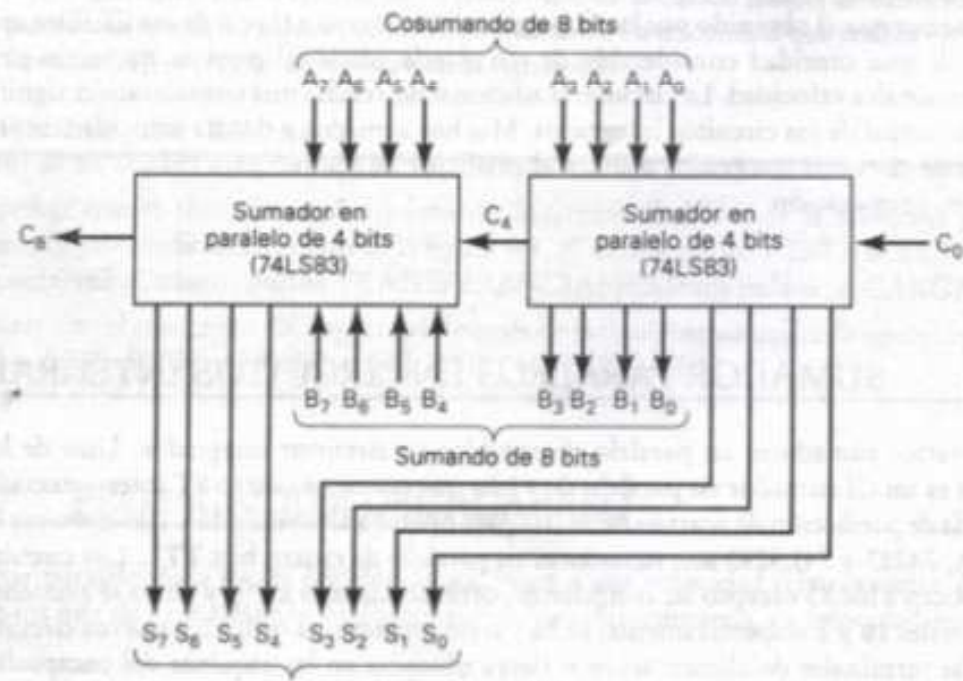


(a) Sumador en paralelo completo de 4 bits con registros; (b) señales empleadas para sumar números binarios que están en la memoria y almacenar el resultado en el acumulador.

(a) Símbolo de bloque para el sumador en paralelo de 4 bits 74LS83; (b) conexión en cascada de dos 74LS83.



(a)



(b)